

GPI8HIRGIC GaN Power IC in DFN5x6 Package

Preliminary Datasheet version: 1.0

Features

BV_{dss}	R_{dson}	I_{ds}
650V	175 m Ω	7.5 A

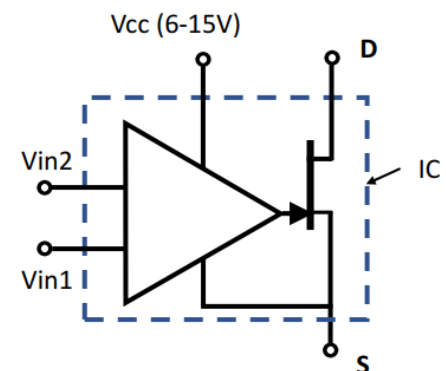
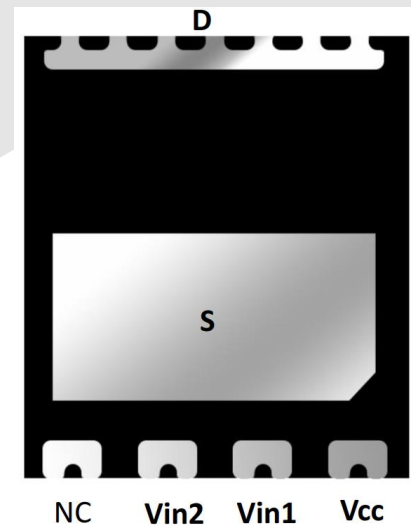
- Edge-triggered high-side power IC
- Small transformer isolation
- Wide Vcc range
- Low Rds and high dv/dt capability
- Extremely low input/output capacitance
- Fast switching
- Low Profile

Applications

- High-side switch in switching power applications
- Power adapters and power delivery chargers

Description

These devices are power IC based on 650 V Power GaN HEMTs using proprietary (US patent pending) E-mode GaN on silicon technology. The gate driver is integrated with the main power transistor resulting in fast switching, high system power density and low cost. Edge triggering narrow pulse is used to control device turn-on/off. This results in high noise immunity and small and inexpensive transformer for isolation and level shifting for the high-side switch in a half bridge application.





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Basic Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	BV_{dss}	Drain-Source breakdown voltage	$V_{gs}=0V$ $I_d=10\mu A$		650		V
2	R_{dson}	Static drain-source on resistance, $T_C = 25^\circ C$	$V_{gs}=6V$ $I_d=1.8A$	165	175	300	$m\Omega$
3	Vcc	Drive supply voltage		6	10	15	V
4	Vin1	Turn-off narrow pulse triggering pulse	Pulse width 50ns-300ns	2.5	5	8	V
5	Iin1	Turn-off current	Pulse width 50ns-300ns		0.02		mA
6	Ciss1	Input capacitance			0.3		pF
7	Qg1	Input gate charge			6.5		fC
8	Vin2	Turn-on narrow pulse triggering pulse	Pulse width 50ns-300ns	2.5	5	8	V
9	Iin2	Turn-off current	Pulse width 50ns-300ns		0.02		mA
10	Ciss2	Input capacitance			0.3		pF
11	Qg2	Input gate charge			6.5		fC
Switching Performance				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$t_{d(on)}$	Turn-on delay time	$V_{ds}=385V$ $I_d=1.6A$ $V_{in1/2}=5V$ $V_{dd}=6.5V$		15		ns
2	t_r	Vds rise time (turn-off)			8		ns
3	$t_{d(off)}$	Turn-off delay time			10		ns
4	t_f	Vds Fall time (turn-on)			12		ns

Device Characteristics

For more information, visit us at: www.iganpower.com, or contact us at sales@iganpower.com

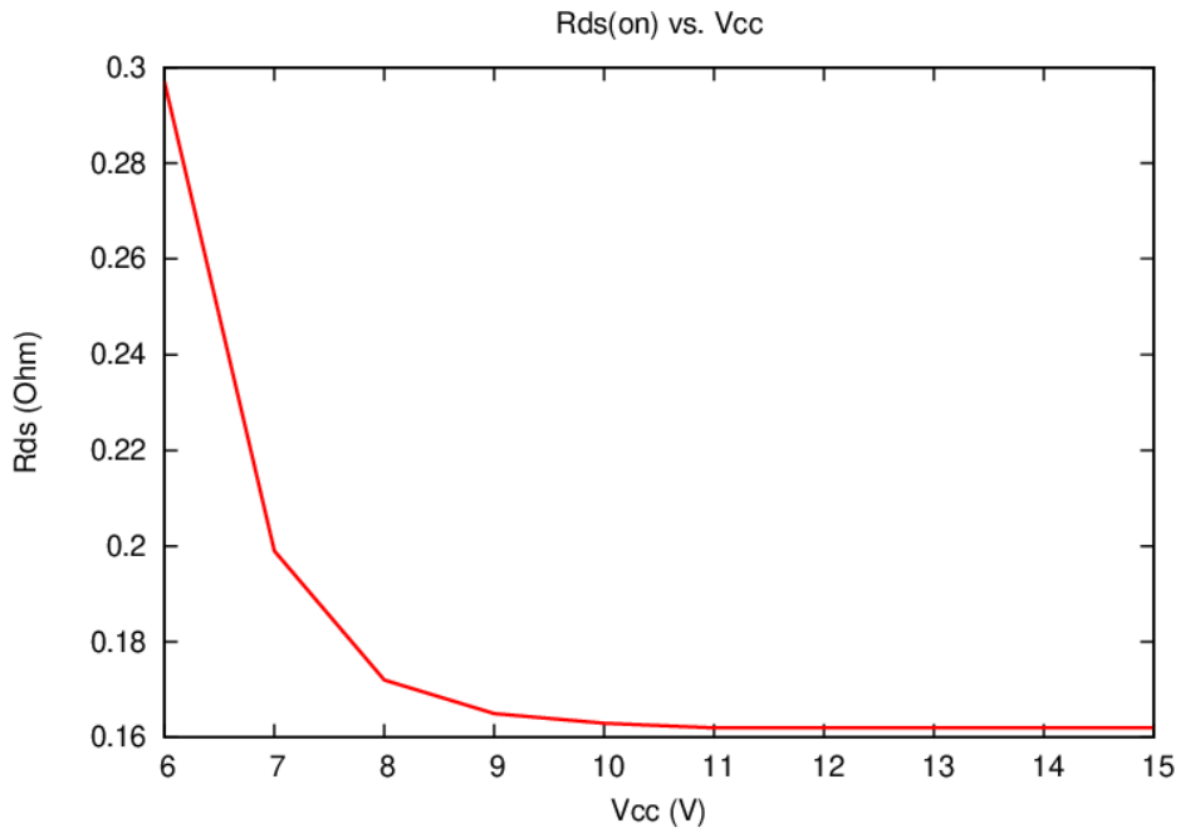


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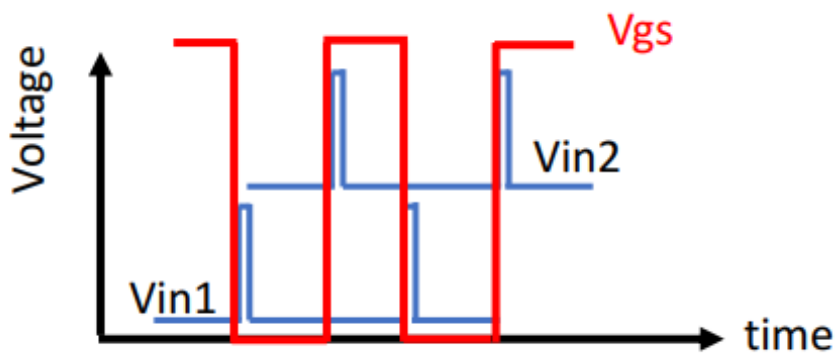
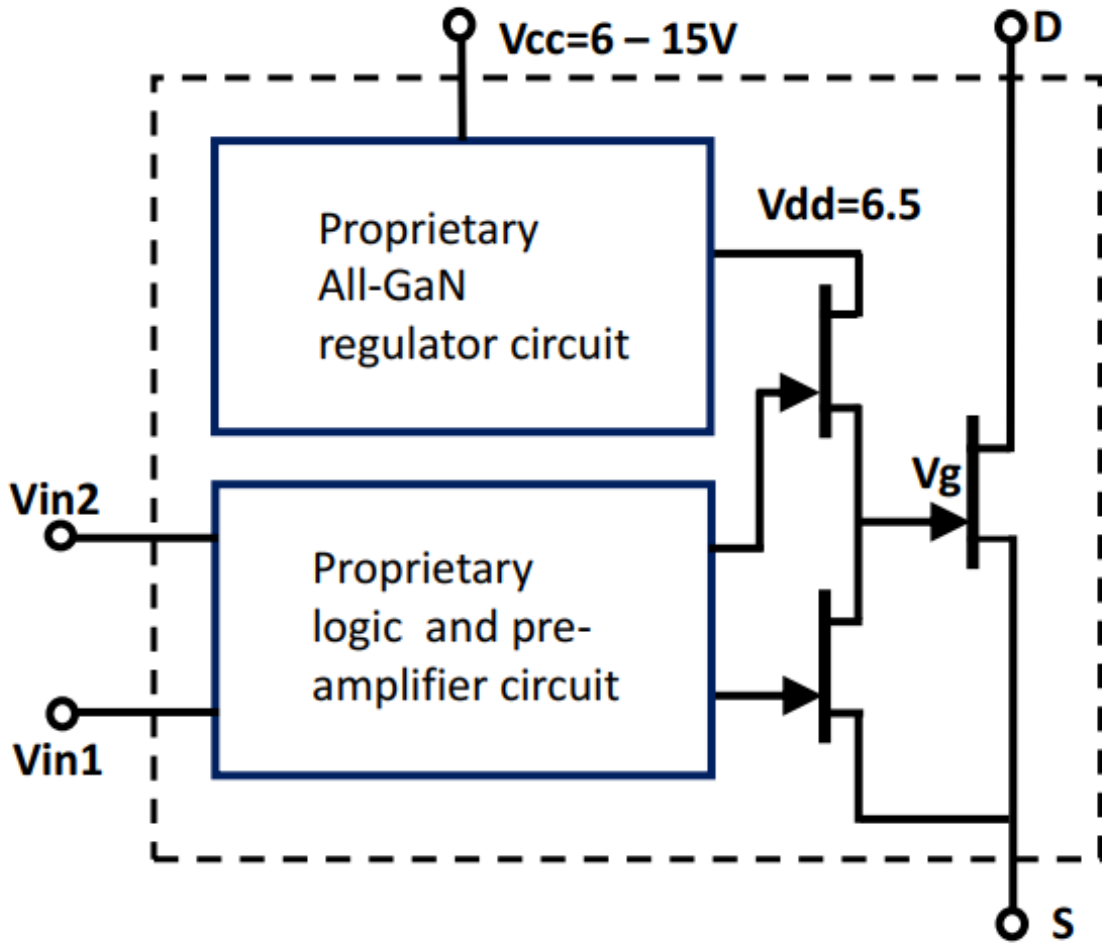
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Electrical Performance

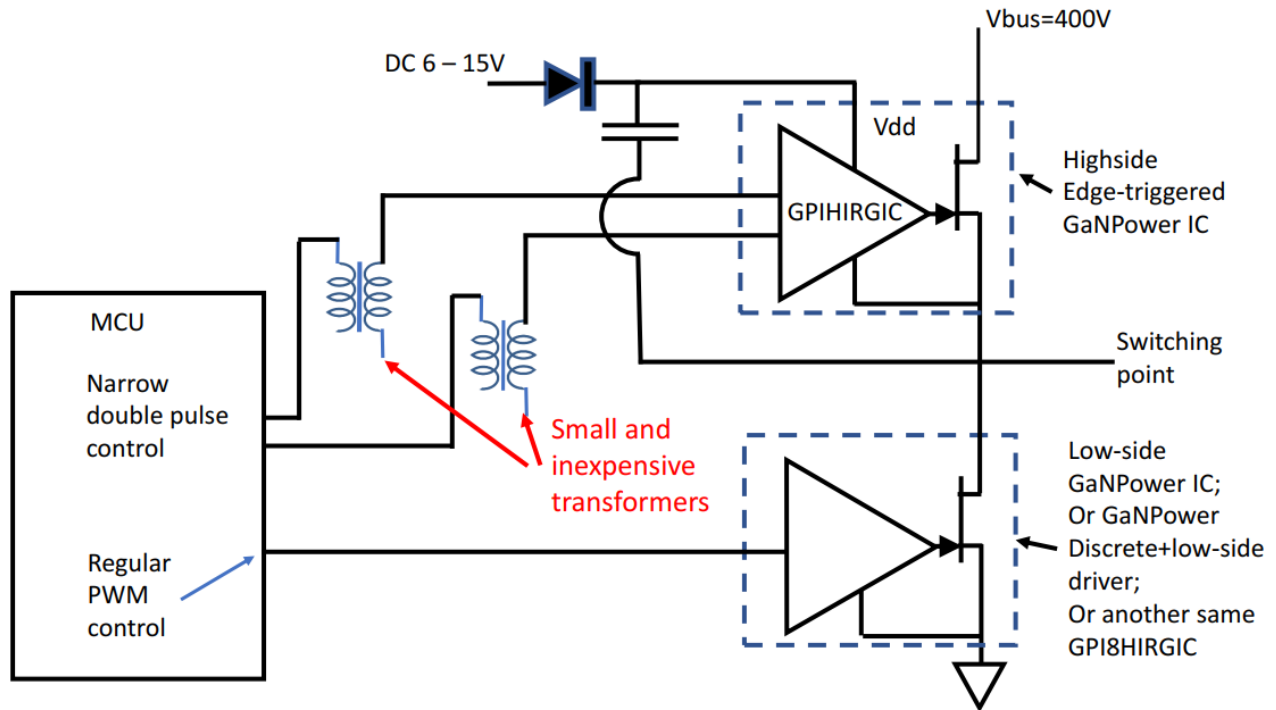
Rds(on) vs. Vdd at Id=15mA



Internal Schematic and waveforms



Typical Application Circuit (Conceptual)

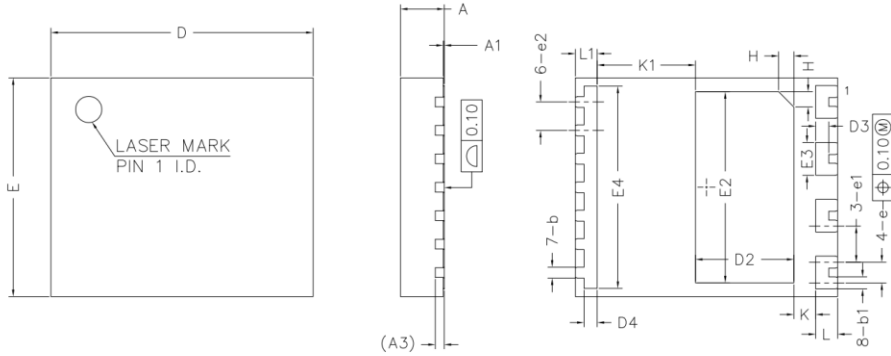




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Package Information



COMMON DIMENSIONS
 (UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
A3	0.203REF		
b	0.20	0.25	0.30
b1	0.225	0.275	0.325
D	5.90	6.00	6.10
E	4.90	5.00	5.10
D2	2.15	2.25	2.35
E2	4.27	4.37	4.47
D3	0.20	0.30	0.40
E3	0.65	0.75	0.85
D4	0.20	0.30	0.40
E4	4.525	4.625	4.725
e	0.375	0.475	0.575
e1	0.725	0.825	0.925
e2	0.55	0.65	0.75
H	0.35REF		
K	0.35	0.50	0.65
K1	2.10	2.25	2.40
L	0.40	0.50	0.60
L1	0.40	0.50	0.60



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GaN HEMT Frequently Asked Questions

1	<p>Q: Can we do pin to pin switch for silicon MOSFET or IGBT?</p> <p>A: The short answer is no. GaN HEMT power devices are far superior than the best silicon devices such as super junction MOSFETs. However, due to different requirements of gate driving voltage and extremely high dv/dt slew rate, special drivers and optimized PCB layouts are recommended to minimize the impact from circuit parasitics. Some packaging forms such as GaNPower's DFN packaged devices offer both sense and force for the source terminal. Also, for traditional TO220 packages, please be advised that the pins are arranged as Gate – Source -Drain, and the thermal pad is connected to the source instead of drain.</p>
2	<p>Q: Are GaN power devices reliable?</p> <p>A: GaN power HEMTs have been tested by GaNPower and many other vendors, users and testing facilities to be as reliable (if not better than) silicon counterparts.</p>
3	<p>Q: How do GaN power devices compare with SiC?</p> <p>A: Currently GaN power HEMT devices are most suitable for low to medium voltage ($\leq 1200V$) and power (<50KW) applications.</p>
4	<p>Q: Do we need to parallel an FRD for applications such as inverters?</p> <p>A: GaN devices are different from silicon MOSFET or IGBT in that they have no inherent PN junction diodes that cause reverse recovery issue. User do not need to parallel an FRD for the purpose of suppressing the body diode reverse recovery effect, since GaN HEMT can operate in both first and third quadrants. However, care should be taken for the dead time power loss since the Vsd voltage of GaN HEMT is usually close to 2V. This is especially true when a negative gate voltage is applied.</p>
5	<p>Q: Can we parallel GaN HEMT devices?</p> <p>A: Yes, GaN HEMT is ideal for paralleling, due to positive temperature coefficient of Rds(on) and slightly positive temperature coefficient of threshold voltage.</p>